

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> ( Not for submission under 37 CFR 1.99)	Application Number		10629301
	Filing Date		2003-07-28
	First Named Inventor	Lewis B. Aronson	
	Art Unit	2613	
	Examiner Name	Kenneth J. Malkowski <i>Phan, Hanh</i>	
Attorney Docket Number		15436.247.2.1.3	

/HP/	1	GREEN, MICHAEL, et al., "Mixing it up with OC-192 CMOS Transceivers", CommsDesign, An EE Times Community, 8 pgs, 03 May 2006, available at: <a href="http://www.commsdesign.com/main/2000/12/0012feat6.htm">http://www.commsdesign.com/main/2000/12/0012feat6.htm</a>	<input type="checkbox"/>
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/HP/	3	Dallas Semiconductor, "MAX3872 Multirate Clock and Data Recovery with Limiting Amplifier," 2 pages, March 30, 2003, available at: <a href="http://www.maxim-ic.com/quick_view2.cfm/qv_pk/3705">http://www.maxim-ic.com/quick_view2.cfm/qv_pk/3705</a>	<input type="checkbox"/>
/HP/	4	Huiqing Zhong and Stephen I. Long, "Monothic Clock and Data Recovery Chip for 10GB/S Fiber Communications Systems," 4 pages 1997-98.	<input type="checkbox"/>
/HP/	5	GIGA an Intel Company, "2.5 Gbit/s Clock and Data Recovery GD16546B," 9 pages, July 31, 2001.	<input type="checkbox"/>

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Examiner Signature	/Hanh Phan/	Date Considered	08/06/2007
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Applicant: Lewis B. Aronson et al.

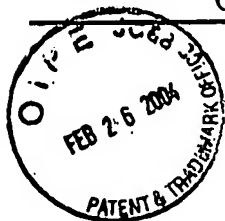
Confirmation No.: 6453

Serial No.: 10/629,301

Att'y Docket No.: 15436.247.2.1.3

Filing Date: July 28, 2003

Group: 2811

For: TRANSCEIVER MODULE AND INTEGRATED CIRCUIT WITH MULTI-RATE EYE  
OPENERS AND BYPASSINFORMATION DISCLOSURE CITATIONS MADE BY APPLICANTU.S. Patent Documents

<u>Examiner Initial*</u>	<u>Document Number</u>	<u>Issue Date</u>	<u>Name</u>
/HP/ 1	5,854,704	12/29/1998	Grandpierre
/HP/ 2	6,256,127 B1	07/03/2001	Taylor
/HP/ 3	4,932,038	06/05/1990	Windus
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/HP/ 6	2003/0053170 A1	03/20/2003	Levinson et al.

Foreign Patent Documents

<u>Examiner Initial*</u>	<u>Document Number</u>	<u>Publication Date</u>	<u>Country or Patent Office</u>	<u>Translation</u>
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Other Documents

(including author, title, pertinent pages, etc.)

<u>Examiner Initial*</u>	
/HP/ 7	LXT16706/16707 SerDes Chipset, Intel Products, www.intel.com/design/network/products/optical/phys/lxt16706.htm, April 19, 2002.
/HP/ 8	LXT35401 XAUI-to-Quad 3.2G Transceiver, Intel Products, www.intel.com/design/network/products/optical/phys/lxt35401.htm, April 19, 2002.

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- /HP/ 9 Texas Instruments User's Guide, *TLK2201 Sedes EVM Kit Setup and Usage*, Mixed Signal DSP Solutions, July 2000.
- /HP/ 10 Texas Instruments User's Guide, *TLK1501 Serdes EVM Kit Setup and Usage*, Mixed Signal Products, June 2000.
- /HP/ 11 National Semiconductor DS92LV16 Design Guide, *Serializing Made Simple*, February 2002.
- /HP/ 12 Vaishali Semiconductor, *Fibre Channel Transceiver*, VN16117, MDSN-0002-02, 08/09/2001.
- /HP/ 13 Fairchild Semiconductor, Application Note 77, *CMOS, the Ideal Logic Family*, January 1983.
- /HP/ 14 Analog Target Specification, Annex 48B, Published by IEEE New York, 05/2001, pp. 6-14.

### References Cited by Applicants

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The reference designations "A1," "A2," etc. (referring to Applicant's reference 1, Applicant's reference 2, etc.) will be used by the Examiner in the same manner as Examiner's reference designations "A," "B," "C," etc. on Office Action Form PTO-1142.

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